ABSTRACT

A pair of pads is formed on an insulating layer formed on a top surface of a substrate, and a plurality of through-holes is laid out at equal intervals between the pads. Adjoining through holes are connected alternately by upper-layer wire interconnect lines exposed on the insulating layer or lower-layer wire interconnect lines buried in the insulating layer, thus constituting a check pattern. A DC power supply is connected between the pair of pads, and a constant current is supplied to a chain pattern of the through holes. Two probes move on a chip surface along the chain pattern of the through holes while keeping a given interval spacing. The probes sequentially scan the upper-layer wire interconnect lines exposed through the chip surface of the chain pattern of the through-holes.